

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY GURAJADA VIZIANAGARAM
IV B. Tech I Semester Regular/Supplementary Examinations OCT/NOV 2025
DIGITAL IC DESIGN USING CMOS

(ECE)

Time: 3 hours

Max. Marks: 70

Answer any **FIVE** Questions. **ONE** Question from **Each unit**

All Questions Carry Equal Marks

UNIT-I

1. a) Explain the working principle of a Pseudo NMOS Inverter. Derive expressions for its threshold voltage [7M]
 b) Explain the effect of transistor sizing on voltage levels, threshold voltage, and switching characteristics in pseudo NMOS circuits. [7M]
- (OR)
2. a) Compare and contrast CMOS inverter logic with pseudo NMOS logic in terms of structure, performance, and power consumption. [7M]
 b) Explain how AND, OR, and NOR gates are implemented using pseudo NMOS logic. [7M]

UNIT-II

3. a) Design a CMOS circuit to realize the Boolean function $y = (a + b)(c + d)$ [7M]
 b) Compare NMOS, CMOS, and Transmission Gate logic families in terms of design, performance, and power consumption. [7M]
- (OR)
4. a) Explain the design and operation of a CMOS Full Adder circuit. Derive its logic equations and transistor-level realization. [7M]
 b) Explain the design of complex CMOS logic circuits to realize Boolean expressions. [7M]

UNIT-III

5. a) Design a CMOS positive edge-triggered D flip-flop using transmission gates. [7M]
 b) Compare SR latch, D latch, and D flip-flop in terms of structure, functionality, and applications. [7M]
- (OR)
6. a) Explain the behavior of bistable elements in MOS logic circuits. [7M]
 b) Discuss the concept of clocked latch and flip-flop circuits. [7M]

UNIT-IV

7. a) Explain the operation of Domino CMOS logic circuits. [7M]
 b) Explain the basic principle and operation of Dynamic Logic Circuits. [7M]
- (OR)
8. a) Derive and explain the voltage bootstrapping technique in dynamic MOS logic circuits. [7M]
 b) Compare Static CMOS Logic and Dynamic CMOS Logic in terms of design, operation, and performance. [7M]

UNIT-V

9. a) Compare DRAM, SRAM, and Flash Memory in terms of operation, density, speed, and applications. [7M]
 b) Explain the resistive parasitics in interconnects. [7M]
- (OR)
10. a) Differentiate between NOR Flash and NAND Flash memory. [7M]
 b) Write a detailed note on advanced interconnect techniques used in modern VLSI design. [7M]
